**Cell Description:**This is a standard TIELO cell. The purpose of this cell is to hardcode a logic low signal. It is described by the following Boolean equation.

**Truth Table:**

|  |
| --- |
| **Y** |
| 0 |

**Behavioral Verilog:**

//Verilog HDL for "Lib6710\_06", "TIELO" "behavioral"

module TIELO ( Y );

output Y;

assign Y = 1'b0;

endmodule

**Cell Size:**

|  |  |  |
| --- | --- | --- |
| **Drive Strength** | **Height (μM)** | **Width (μM)** |
| TIELO | 27.0 | 4.8 |

**Logic Symbol:**

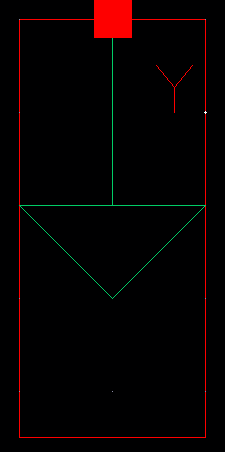
****

Figure 1: Symbol View for the TIELO cell.

**CMOS Schematic:**

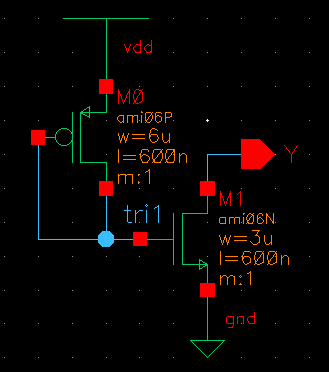
****

Figure 2:

**CMOS Layout:**

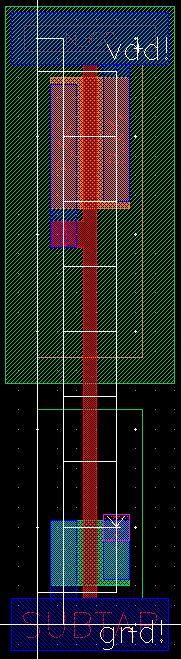
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Figure 3: CMOS layout for the TIELO cell